

## CLAIMS

What is claimed is:

- 1           1.       A method comprising:  
2       accessing a label stack of a received packet, the label stack including a plurality of  
3           multiprotocol label switching (MPLS) labels;  
4       reading from an incoming label mapping (ILM) table stored in a first memory an entry  
5           associated with a top MPLS label in the label stack and a number of other entries;  
6       storing the number of other entries read from the ILM table in a second memory.
- 1           2.       The method of claim 1, further comprising performing an action  
2       associated with the top MPLS label.
- 1           3.       The method of claim 2, further comprising:  
2       accessing one of the number of other ILM entries stored in the second memory, the one  
3           ILM entry associated with a next MPLS label in the label stack; and  
4       performing an action associated with the next MPLS label.
- 1           4.       The method of claim 1, further comprising:  
2       reading from the ILM table stored in the first memory a number of additional entries; and  
3       storing in the second memory the additional number of ILM entries read from the first  
4       memory.
- 1           5.       The method of claim 1, wherein the plurality of MPLS labels of the label  
2       stack are in sequence.
- 1           6.       The method of claim 1, wherein the plurality of MPLS labels of the label  
2       stack are out of sequence.
- 1           7.       The method of claim 6, wherein the ILM table comprises a hash table.

1           8.     The method of claim 1, wherein the first memory comprises an external  
2 memory and the second memory comprises an on-chip memory.

1           9.     The method of claim 1, wherein the first memory comprises part of an on-  
2 chip memory subsystem coupled with a processing engine, and wherein the second  
3 memory comprises an on-chip memory associated with the processing engine.

1           10.    A device comprising:  
2 a processing system; and  
3 an on-chip memory coupled with the processing system;  
4 wherein the processing system is programmed to perform operations including  
5                accessing a label stack of a received packet, the label stack including a  
6                plurality of multiprotocol label switching (MPLS) labels;  
7                reading from an incoming label mapping (ILM) table stored in a second  
8                memory an entry associated with a top MPLS label in the label  
9                stack and a number of other entries;  
10              storing the number of other entries read from the ILM table in the on-chip  
11              memory.

1           11.    The device of claim 10, wherein the processing system is programmed to  
2 perform operations further comprising performing an action associated with the top  
3 MPLS label.

1           12.    The device of claim 11, wherein the processing system is programmed to  
2 perform operations further comprising:  
3 accessing one of the number of other ILM entries stored in the on-chip memory, the one  
4 ILM entry associated with a next MPLS label in the label stack; and  
5 performing an action associated with the next MPLS label.

1           13.     The device of claim 10, wherein the processing system is programmed to  
2 perform operations further comprising:  
3 reading from the ILM table stored in the second memory a number of additional entries;  
4           and  
5 storing in the on-chip memory the additional number of ILM entries read from the second  
6           memory.

1           14.     The device of claim 10, wherein the plurality of MPLS labels of the label  
2 stack are in sequence.

1           15.     The device of claim 10, wherein the plurality of MPLS labels of the label  
2 stack are out of sequence.

1           16.     The device of claim 15, wherein the ILM table comprises a hash table.

1           17.     The device of claim 10, wherein the second memory comprises another  
2 on-chip memory coupled with the processing system.

1           18.     The device of claim 10, wherein the second memory comprises an external  
2 memory.

1           19.     The device of claim 10, wherein the processing system comprises one of a  
2 number of processing engines.

1           20.     The device of claim 19, wherein the on-chip memory comprises part of the  
2 one processing engine.

1           21.     The device of claim 19, wherein the on-chip memory comprises a memory  
2 subsystem coupled with the number of processing engines.

1           22.    An apparatus comprising:  
2    a memory; and  
3    a processing device coupled with the memory, the processing device including a  
4       processing system and an on-chip memory coupled the processing system;  
5    wherein the processing system is programmed to perform operations including  
6       accessing a label stack of a received packet, the label stack including a  
7       plurality of multiprotocol label switching (MPLS) labels;  
8       reading from an incoming label mapping (ILM) table stored in the  
9       memory an entry associated with a top MPLS label in the label  
10      stack and a number of other entries;  
11      storing the number of other entries read from the ILM table in the on-chip  
12      memory.

1           23.    The apparatus of claim 22, wherein the processing system is programmed  
2    to perform operations further comprising performing an action associated with the top  
3    MPLS label.

1           24.    The apparatus of claim 23, wherein the processing system is programmed  
2    to perform operations further comprising:  
3    accessing one of the number of other ILM entries stored in the on-chip memory, the one  
4       ILM entry associated with a next MPLS label in the label stack; and  
5    performing an action associated with the next MPLS label.

1           25.    The apparatus of claim 22, wherein the processing system is programmed  
2    to perform operations further comprising:  
3    reading from the ILM table stored in the memory a number of additional entries; and  
4    storing in the on-chip memory the additional number of ILM entries read from the  
5    memory.

1           26.     The apparatus of claim 22, wherein the plurality of MPLS labels of the  
2     label stack are in sequence.

1           27.     The apparatus of claim 22, wherein the plurality of MPLS labels of the  
2     label stack are out of sequence.

1           28.     The apparatus of claim 27, wherein the ILM table comprises a hash table.

1           29.     The apparatus of claim 22, wherein the processing system comprises one  
2     of a number of processing engines.

1           30.     The apparatus of claim 29, wherein the on-chip memory comprises part of  
2     the one processing engine.

1           31.     The apparatus of claim 29, wherein the on-chip memory comprises a  
2     memory subsystem coupled with the number of processing engines.

1           32.     An article of manufacture comprising:  
2     a machine accessible medium providing content that, when accessed by a machine,  
3     causes the machine to  
4             access a label stack of a received packet, the label stack including a plurality of  
5             multiprotocol label switching (MPLS) labels;  
6             read from an incoming label mapping (ILM) table stored in a first memory an  
7             entry associated with a top MPLS label in the label stack and a number of  
8             other entries;  
9             store the number of other entries read from the ILM table in a second memory.

1           33.     The article of manufacture of claim 32, wherein the content, when  
2     accessed, further causes the machine to perform an action associated with the top MPLS  
3     label.

1           34.     The article of manufacture of claim 33, wherein the content, when  
2     accessed, further causes the machine to:  
3     access one of the number of other ILM entries stored in the second memory, the one ILM  
4     entry associated with a next MPLS label in the label stack; and  
5     perform an action associated with the next MPLS label.

1           35.     The article of manufacture of claim 32, wherein the content, when  
2     accessed, further causes the machine to:  
3     read from the ILM table stored in the first memory a number of additional entries; and  
4     store in the second memory the additional number of ILM entries read from the first  
5     memory.

1           36.     The article of manufacture of claim 32, wherein the plurality of MPLS  
2     labels of the label stack are in sequence.

1           37.     The article of manufacture of claim 32, wherein the plurality of MPLS  
2     labels of the label stack are out of sequence.

1           38.     The article of manufacture of claim 37, wherein the ILM table comprises a  
2     hash table.

1           39.     The article of manufacture of claim 32, wherein the first memory  
2     comprises an external memory and the second memory comprises an on-chip memory.

1           40.     The article of manufacture of claim 32, wherein the first memory  
2     comprises part of an on-chip memory subsystem coupled with a processing engine, and  
3     wherein the second memory comprises an on-chip memory associated with the  
4     processing engine.

1           41.    A system comprising:  
2    a system memory coupled with a bus;  
3    a program memory coupled with the bus, the program memory to store a set of  
4       instructions; and  
5    a processing device coupled with the bus, the processing device including a processing  
6       system and an on-chip memory coupled the processing system;  
7    wherein the processing system, when executing the set of instructions, performs  
8       operations including  
9        accessing a label stack of a received packet, the label stack including a  
10        plurality of multiprotocol label switching (MPLS) labels;  
11        reading from an incoming label mapping (ILM) table stored in the system  
12        memory an entry associated with a top MPLS label in the label  
13        stack and a number of other entries;  
14        storing the number of other entries read from the ILM table in the on-chip  
15        memory.

1           42.    The system of claim 41, wherein the processing system, when executing  
2    the set of instructions, performs operations further comprising performing an action  
3    associated with the top MPLS label.

1           43.    The system of claim 42, wherein the processing system, when executing  
2    the set of instructions, performs operations further comprising:  
3    accessing one of the number of other ILM entries stored in the on-chip memory, the one  
4       ILM entry associated with a next MPLS label in the label stack; and  
5    performing an action associated with the next MPLS label.

1           44.     The system of claim 41, wherein the processing system, when executing  
2     the set of instructions, performs operations further comprising:  
3     reading from the ILM table stored in the system memory a number of additional entries;  
4           and  
5     storing in the on-chip memory the additional number of ILM entries read from the  
6     memory.

1           45.     The system of claim 41, wherein the plurality of MPLS labels of the label  
2     stack are in sequence.

1           46.     The system of claim 41, wherein the plurality of MPLS labels of the label  
2     stack are out of sequence.

1           47.     The system of claim 46, wherein the ILM table comprises a hash table.

1           48.     The system of claim 41, wherein the program memory comprises a read  
2     only memory (ROM).

1           49.     A method comprising allocating a number of multiprotocol label  
2     switching (MPLS) labels for a local forwarding equivalence class (FEC) at an edge node  
3     of an MPLS domain in sequence.

1           50.     The method of claim 49, wherein the edge node supports a number of  
2     local FECs, the method further comprising maintaining a separate label space for each  
3     local FEC.

1           51.     The method of claim 49, further comprising allocating at least some of the  
2     MPLS labels associated with the local FEC in ascending order from an outermost tunnel  
3     to an innermost tunnel.